

SilAx™

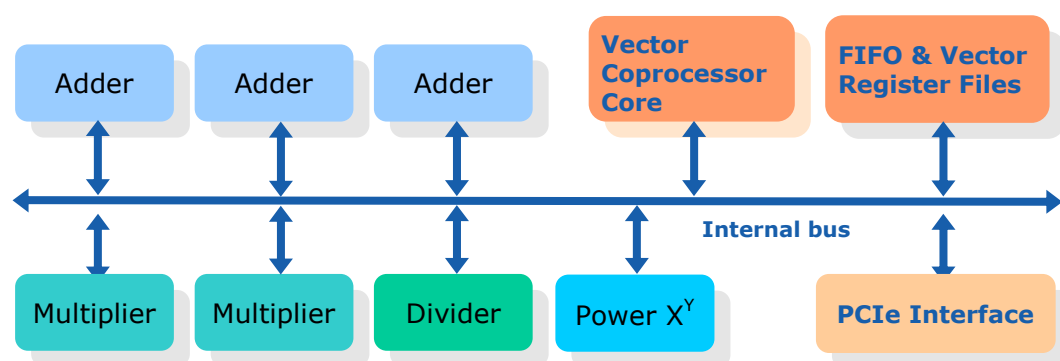
DFPA Hardware Accelerator Cards

Architecture

SilAx™ is a customizable FPGA-based DFPA (Decimal Floating Point Arithmetic) hardware accelerator card that connects to the server's standard four-lane (or higher) PCIe interface. The accelerator card is accompanied by a C-language API functions library to handle the IEEE 754-2008 standard arithmetic operations in vector form and have them passed directly to the hardware accelerator.

The core execution control of SilAx™ is carried by the Vector Coprocessor, which process decimal operations on large number of vector operands passed by the CPU to the FIFO buffer via DMA. Vector Register Files are used to store large number of operands and resultants during execution of decimal operations.

Arbitrary combinations of core arithmetic units are implemented on the FPGA, whose relative numbers are optimized according to the application decimal arithmetic portfolio.



A sample SilAx FPGA implementation

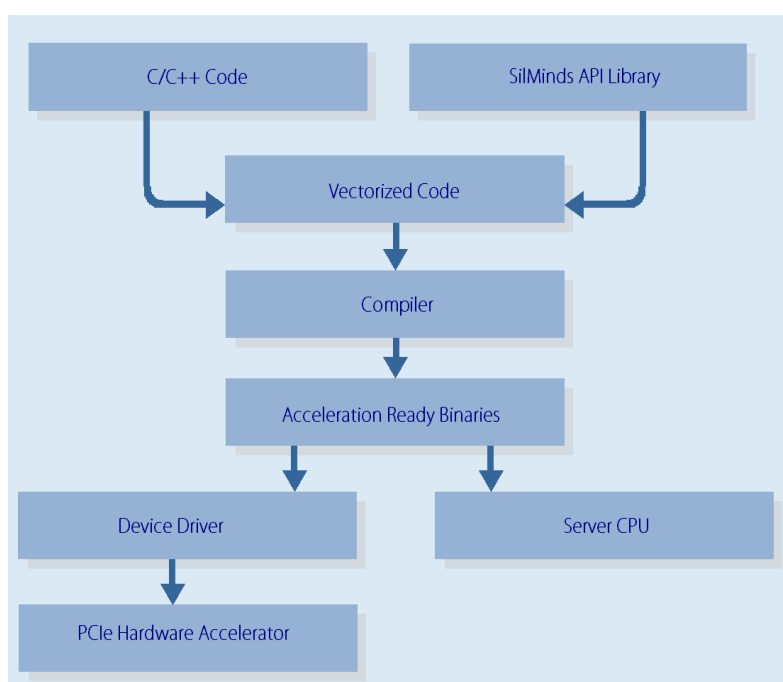
Code adaptation & flow

Using the associated C-extension API, SilMinds works with the client to analyze the application source code and to vectorize it.

When running the adapted code executable, all decimal arithmetic operations that are then implemented using SilAx API functions are directed to the SilAx card via the PCIe interface.

The diagram to the right illustrates the steps of the application adaptation as well as the logical flow of the re-compiled application executable.

SilMinds will provide training and technical support to get the full contracted functionality implemented and operational.



SilAx™ 1.0 Card Features & Options

- ◆ Board: PLDA XpressLX330T
- ◆ Interface & I/O protocols
 - PCIe 2.0 (2.5 GB/S over 8x Gen-1)
 - PCI-SIG compliant
- ◆ FPGA
 - Xilinx Vertex-5 LX330T
 - 125 MHz clock rate
 - Up to 330 K Lookup Tables (LUTs)
- ◆ Core units (64 and 128 bits)
 - Adder, multiplier, Fused-multiplier-adder, divider, square rooter, power, decimal-string cross converter
 - Configurable arrangement of arithmetic core unit combinations or pipes
- ◆ Vector coprocessor
 - 128 instructions; with both 64-bit and 128-bit operand support
 - Parameterized vector register size that could be set to order of thousand vectors
 - 4 KB program cache
 - Multiple execution pipes may be configured to support several concurrent application instances
- ◆ 4 KB FIFO, for input-output buffering of both instructions and operand/resultant vectors
- ◆ Vector Register File: Up to 32 vector and 32 scalar operand registers (configurations with fewer operand registers are available at lower cost)
- ◆ Speedup
 - Per application thread: speedup anywhere from 2x to 20x, inclusive of I/O overhead
 - Exact speedup depends mainly on the percent of application's DFP operations
 - DFP computation (execution) speedup up to order of 100x (hundreds), i.e. support of multiple application instances over multiprocessing and virtualized environments
- ◆ Supported server sizes
 - Riser card provided for 1U and 2U enclosures
 - Directly pluggable into 4U rack-mounted or standalone servers
- ◆ Power supply through ATX HDD AMP connector



C-extension API

SilAx™ is supplied with an extendable C-based API that contains over 140 functions to implement about a dozen decimal arithmetic operations and support other requirements such as memory management and exception handling.

- Flexible memory allocation with memory lock
- Macro based implementation to preserve compilation and run time speed, with fewer lines of code
- All operations support both 64-bit and 128-bit operands
- Portable code that can be used over any platform (by only editing data types header file)
- 100+ decimal arithmetic operations (Add, Subtract, Multiply, Divide, Fused Multiply Add, , Square root, Power, Log, Increment, Round, Quantize, ...), in addition to cross-decimal-string conversion
- 15 memory transfer operations (Load, Store, Copy and Conditional Copy)
- 18 Trap and Flag Handling operations (Clear, Set, Get, Enable, Disable, Swap)

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