SILMINDS
SILICON FOR GREEN COMPUTING

IP Core Product Data Sheet

DFP Newton-Raphson Square Root Units
NRDecDiv64/128

NRDecSqrt64 and **NRDecSqrt128** IP core units are DFP Square Root designs, offered in 64-bit and 128-bit versions. The unit computes the square root of a vector Operand. Inputs are encoded in Decimal Interchange Format**.**

The square root unit is based on the Newton-Raphson iterative method. It computes the final result in 2 iterations for the 64-bit version and in 3 iterations for the 128-bit version. The product is fully compliant with the IEEE 754-2008 Standard.

Key Features

⇒ Full IEEE 754-2008 compliance
⇒ Decimal128 (34 decimal digits) format support
⇒ Decimal Interchange format with Densely Packed Decimal (DPD) encoding support
⇒ Seven rounding modes support
⇒ Result is available at every clock cycle
⇒ Overflow, Underflow, Invalid, and Inexact operation flags
⇒ Tested with over 500,000 test cases compliant with IEEE 754-2008 format
⇒ Full DFP accuracy and precision support
⇒ Fully synthesizable with no internal tri-states

Performance Data

The table below summarizes gate-level synthesized performance data in TSMC 90 nm, for sample combinational designs. More detailed performance data can be found in the product technical documentation.

Design	Cycle Delay		Nr. of Cycles	Area	
	nS	*FO4*		*μm^2*	*NAND2*
NRDecSqrt64-comb	2.80	62.22	15	443,915.6	157,284
NRDecSqrt128-comb	3.55	78.11	18	975,512.5	345,633

Applications

⇒ DFPA units for next generation processors
⇒ DFPA on-chip co-processors
⇒ DFPA accelerator boards

IP Deliverable

Deliverable depends on the type of licensing agreement and the negotiated business model. The following items could be included:

⇒ Source code:
  - VHDL source code
  - VERILOG source code
  - Encrypted or plain text EDIF netlist
⇒ FPGA code versions, optimized for either speed or area
⇒ VHDL & VERILOG test bench environments
⇒ Full test suites compliant with IEEE 754-2008 standard.
⇒ Technical documentation
⇒ HDL core specification
⇒ Synthesis scripts
⇒ IP Core implementation support

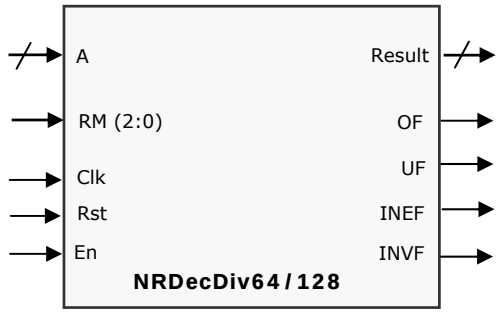
Configurations

NRDecSqrt64/128 can be combined with other SilMinds IP core units to comprise arbitrary decimal coprocessor architectures. Deployment is made easy and reliable through a compact core size, parameterized RTL, and flexible test benches.

Product Verification

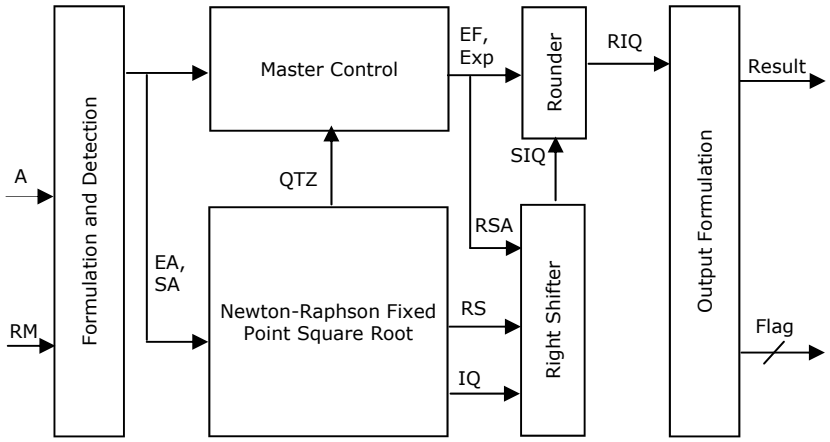
This product has been verified using an innovative and efficient constraint driven test vector generation tool. The test vectors cover all valid cases in conformance with the IEEE 754-2008 standard.

Symbol & Block Diagram



Inputs	
A	Dividend
B	Divisor
RM	Rounding Mode
Clk	System Clock
Rst	System Reset
En	Enable

Outputs	
Result	Resultant
OF	Overflow Flag
UF	Underflow Flag
INEF	INExact Flag
INVF	INValid Flag



A	Input
EA	Input Exponent
SA	Input Significand
RS	Remainder Sign
IQ	Intermediate Quotient
RSA	Right Sift Amount
SIQ	Shifted Intermediate Result
RIQ	Rounded Intermediate Result
EF	Exception Flags
Exp	Final Exponent
FQ	Final Quotient
Flags	Output Flags

Square Root Unit Functions

Formulation & Detection

- Decodes input operand using IEEE 754-2008 format to produce the sign bit, significand, and exponent
- Performs special input detection (infinity or NaN)
- Performs significand normalization

Master Control

Generates the result exponent, the output flags, and a number of control signals

Right Shifter

Removes excess trailing zeroes

Rounder

Performs result quotient rounding to fit in the required precision

Fixed Point Divider

- Performs decimal fixed point division ($Q = A/\sqrt{A} = \sqrt{A}$) by calculating the approximate reciprocal ($1/\sqrt{A}$), using Newton-Raphson iterative method
- Employs a novel parallel decimal fixed multiplier to reduce latency

Output Formulation

- Encodes the resultant significand in DPD format
- Formulates the special values (infinity or NaN) to comply with the IEEE 754-2008 standard
- Sets the appropriate flags