SILMINDS
SILICON FOR GREEN COMPUTING

IP Core Product Data Sheet

DFP Fused Multiply-Add Units
DecFMA64/128

DecFMA64 and **DecFMA128** IP core units are first in the market to offer the Fused Multiple-Add function. The FMA unit computes the Multiply-Add operation ±(A×B)±C of three input vector operands. Inputs are encoded in Decimal Interchange Format**.** The product is fully compliant with the IEEE 754-2008 Standard.

Key Features

⇒ Full IEEE 754-2008 compliance
⇒ Decimal128 (34 decimal digits) format support
⇒ Decimal Interchange format with Densely Packed Decimal (DPD) encoding support
⇒ Seven rounding modes support
⇒ Automatic pipelining selectable with arbitrary number of stages
⇒ Result is available at every clock cycle
⇒ Overflow, Underflow, Invalid, and Inexact operation flags
⇒ Tested with over 500,000 test cases compliant with IEEE 754-2008 format
⇒ Full DFP accuracy and precision support
⇒ Fully synthesizable with no internal tri-states

Performance Data

The table below summarizes gate-level synthesized performance data in TSMC 90 nm. More detailed performance data can be found in the product technical documentation.

Design	Cycle Delay		Area	
	nS	*FO4*	*μm^2*	*NAND2*
DecFMA64	6.5	144.4	235,446.1	83,421
DecFMA128	7.0	155.5	471,800.0	167,163

Applications

⇒ DFPA units for next generation processors
⇒ DFPA on-chip co-processors
⇒ DFPA accelerator boards

IP Deliverable

Deliverable depends on the type of licensing agreement and the negotiated business model. The following items could be included:

⇒ Source code:
- VHDL source code
- VERILOG source code
- Encrypted or plain text EDIF netlist

⇒ FPGA code versions, optimized for either speed or area
⇒ VHDL & VERILOG test bench environments
⇒ Full test suites compliant with IEEE 754-2008 standard.
⇒ Technical documentation
⇒ HDL core specification
⇒ Synthesis scripts
⇒ IP Core implementation support

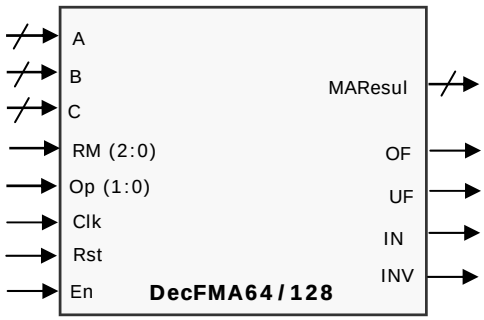
Configurations

DecFMA64/128 can be combined with other SilMinds IP core units to comprise arbitrary decimal coprocessor architectures. Deployment is made easy and reliable through a compact core size, parameterized RTL, and flexible test benches.

Product Verification

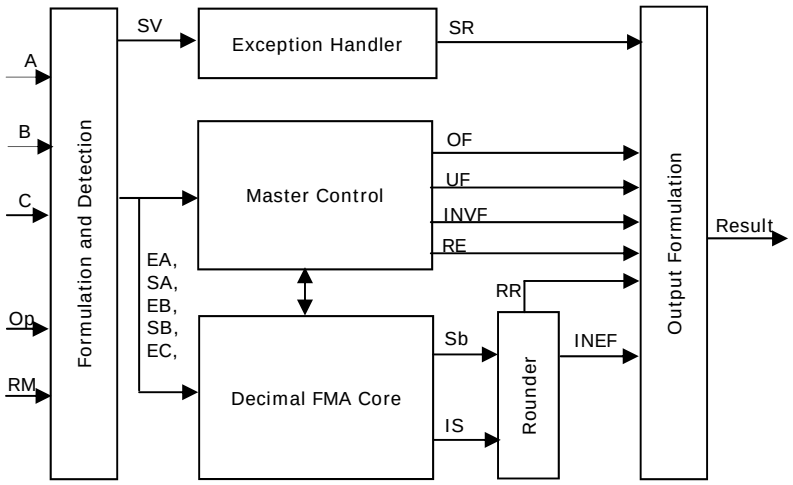
This product has been verified using an innovative and efficient constraint driven test vector generation tool. The test vectors cover all valid cases in conformance with the IEEE 754-2008 standard.

Symbol & Block Diagram



Inputs	
A	Multiplier
B	Multiplicand
C	Addend
RM	Rounding Mode
Op	Operation
Clk	System Clock
Rst	System Reset
En	Enable

Outputs	
Result	Resultant
OF	Overflow Flag
UF	Underflow Flag
INEF	INExact Flag
INVF	INValid Flag



A, B	Multiplicand and Multiplier
C	Addend
Op	Multiply-Add Operation
RM	Rounding Mode
SA, SB, SC	Significand A, B, and C
EA, EB, EC	Exponent A, B, and C
Sb	Sticky bit
IS	Intermediate Sum
SV	Special Value
SR	Special Result
RR	Rounded Result
RE	Result Exponent
INVF	INValid Flag
INEF	INExact Flag
UF	Underflow Flag
OF	Overflow Flag

Fused Multiply-Add Unit Functions

Formulation & Detection

- Decodes input operands (Multiplicand, Multiplier, and Addend) using IEEE 754-2008 format to produce the sign bit, significand, and exponent
- Performs special input detection

Decimal FMA Core

- Performs the multiplication-addition/subtraction operation, where the addition operation is done inherently within the multiplication process, using a parallel fixed-point multiplier with fast decimal carry-propagate adder
- Performs operands alignment
- Calculates the sticky bit

Master Control

- Generates the shift amount needed for operand alignment
- Generates the sticky counter value that determines how many digits to be collected in the sticky bit generator
- Generates the special values (Overflow, Underflow, and Invalid), encodes them, and passes them to output formulation
- Computes the exponent as specified in the IEEE-754-2008 standard

Exception Handler

Handles the exceptions and passes the special results to the output formulation unit

Rounder

- Performs the result rounding operations to fit in the required precision based on the rounding mode, the result's sign, and the shifted result (including a round digit and sticky bit)
- Generates the inexact flag

Output Formulation

- Encodes the resultant significand in DPD format
- Formulates the special values (infinity or NaN) to comply with the IEEE 754-2008 standard
- Sets the appropriate flags