SILMINDS
SILICON FOR GREEN COMPUTING

IP Core Product Data Sheet

DFP Multiplier Units
DecMult64/128

DecMult64 and **DecMult128** IP core units are novel DFP Multiplier designs, offered in 64-bit and 128-bit versions. The Multiplier unit computes the Product of two vector Operands. Inputs are encoded in Decimal Interchange Format**.** The product is fully compliant with the IEEE 754-2008 Standard.

Key Features

⇒ Full IEEE 754-2008 compliance
⇒ Decimal128 (34 decimal digits) format support
⇒ Decimal Interchange format with Densely Packed Decimal (DPD) encoding support
⇒ Seven rounding modes support
⇒ Automatic pipelining selectable with arbitrary number of stages
⇒ Result is available at every clock cycle
⇒ Overflow, Underflow, Invalid, and Inexact operation flags
⇒ Tested with over 500,000 test cases compliant with IEEE 754-2008 format
⇒ Full DFP accuracy and precision support
⇒ Fully synthesizable with no internal tri-states

Applications

⇒ DFPA units for next generation processors
⇒ DFPA on-chip co-processors
⇒ DFPA accelerator boards

IP Deliverable

Deliverable depends on the type of licensing agreement and the negotiated business model. The following items could be included:

⇒ Source code:
- VHDL source code
- VERILOG source code
- Encrypted or plain text EDIF netlist

⇒ FPGA code versions, optimized for either speed or area
⇒ VHDL & VERILOG test bench environments
⇒ Full test suites compliant with IEEE 754-2008 standard.
⇒ Technical documentation
⇒ HDL core specification
⇒ Synthesis scripts
⇒ IP Core implementation support

Performance Data

The table below summarizes gate-level synthesized performance data in TSMC 90 nm, for sample combinational and pipelined designs. The IP core source code is provided with generic parameters to enable automatic pipelining with arbitrary number of pipeline stages. It is noted that the 8-stage pipelined design (of DecMult64) exhibits the best area-delay product among both combinational and pipelined options. More detailed performance data can be found in the product technical documentation.

Design	Delay		Area	
	nS	*FO4*	*μm^2*	*NAND2*
DecMult64-comb	3.55	78.9	185,061	65,569
DecMult64-pipe4	1.05	23.3	243,076	86,124
DecMult64-pipe8	0.62	13.8	314,513	111,435
DecMult128-comb	5.00	111.1	452,585	160,355

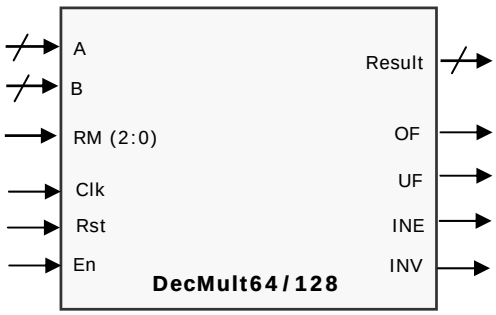
Configurations

DecMult64/128 can be combined with other SilMinds IP core units to comprise arbitrary decimal coprocessor architectures. Deployment is made easy and reliable through a compact core size, parameterized RTL, and flexible test benches.

Product Verification

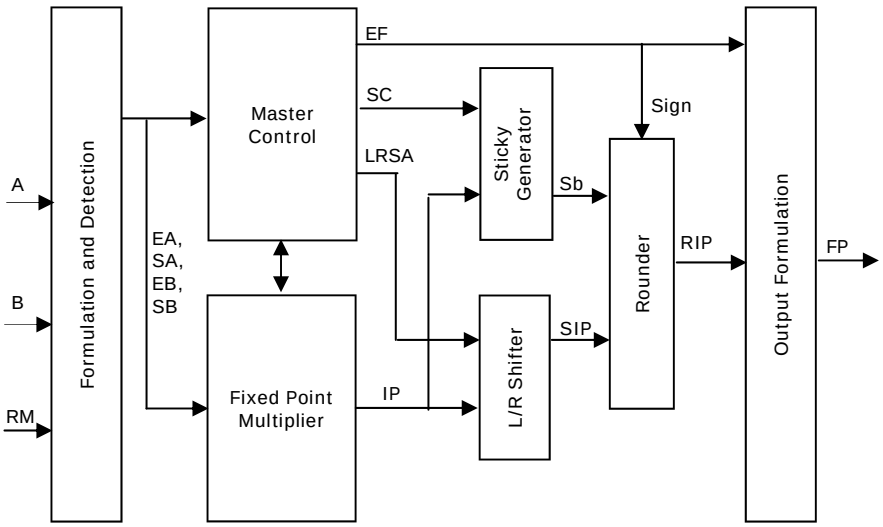
This product has been verified using an innovative and efficient constraint driven test vector generation tool. The test vectors cover all valid cases in conformance with the IEEE 754-2008 standard.

Symbol & Block Diagram



Inputs	
A	Multiplicand
B	Multiplier
RM	Rounding Mode
Clk	System Clock
Rst	System Reset
En	Enable

Outputs	
Result	Resultant
OF	Overflow Flag
UF	Underflow Flag
INEF	INExact Flag
INVF	INValid Flag



A, B	Multiplicand and Multiplier
RM	Rounding Mode
SA, SB	Significands A and B
EA, EB	Exponents A and B
IP	Intermediate Product
SC	Sticky Counter
EF	Exception Flags
Exp	Final Exponent
LRSA	Left/Right Shift Amount
Sb	Sticky bit
SIP	Shifted Intermediate Prod.
RIP	Rounded Intermediate Prod.
FP	Final Product

Multiplier Unit Functions

Formulation & Detection

- Decodes input operands (Multiplicand and Multiplier) using IEEE 754-2008 format to produce the sign bit, significand, and exponent
- Performs special input detection (infinity or NaN)

Master Control

Generates the result exponent, output flags, and a number of control signals

Fixed Point Multiplier

- Performs parallel decimal fixed point multiplication
- Generates partial products using the signed digit recording technique
- Performs partial product reduction
- Employs a novel parallel decimal adder with a Kogge-Stone tree at its final stage

L/R Shifter

Aligns the operands to reach the preferred exponent

Sticky Generator

Determines if rounding is needed as a result of logically ORing all bits to the right of the round digit

Rounder

- Performs the result rounding operations to fit the required precision
- Supports five rounding modes specified in IEEE 754-2008 as well as two additional rounding modes

Output Formulation

- Encodes the resultant significand in DPD format
- Formulates the special values (infinity or NaN) to comply with the IEEE 754-2008 standard
- Sets the appropriate flags