SILMINDS
SILICON FOR GREEN COMPUTING

IP Core Product Data Sheet

DFP Adder Units
DecAdd64/128

DecAdd64 and **DecAdd128** IP core units are novel DFP Adder designs, offered in 64-bit and 128-bit versions. The Adder unit computes the Sum or the Difference of two vector Operands. Inputs are encoded in Decimal Interchange Format**.** The product is fully compliant with the IEEE 754-2008 Standard.

Key Features

⇒ Full IEEE 754-2008 compliance
⇒ Decimal128 (34 decimal digits) format support
⇒ Decimal Interchange format with Densely Packed Decimal (DPD) encoding support
⇒ Seven rounding modes support
⇒ Automatic pipelining selectable with arbitrary number of stages
⇒ Result is available at every clock cycle
⇒ Overflow, Underflow, Invalid, and Inexact operation flags
⇒ Tested with over 500,000 test cases compliant with IEEE 754-2008 format
⇒ Full DFP accuracy and precision support
⇒ Fully synthesizable with no internal tri-states

Performance Data

The table below summarizes gate-level synthesized performance data in TSMC 90 nm, for sample combinational and pipelined designs. The IP core source code is provided with generic parameters to enable automatic pipelining with arbitrary number of pipeline stages. More detailed performance data can be found in the product technical documentation.

Design	Delay		Area	
	nS	*FO4*	*μm^2*	*NAND2*
DecAdd64-comb	2.03	45.1	38,405.1	13,608
DecAdd64-pipe4	0.74	16.4	72,963.3	25,852
DecAdd128-comb	2.55	56.7	71,594.4	25,367

Applications

⇒ DFPA units for next generation processors
⇒ DFPA on-chip co-processors
⇒ DFPA accelerator boards

IP Deliverable

Deliverable depends on the type of licensing agreement and the negotiated business model. The following items could be included:

⇒ Source code:
  - VHDL source code
  - VERILOG source code
  - Encrypted or plain text EDIF netlist
⇒ FPGA code versions, optimized for either speed or area
⇒ VHDL & VERILOG test bench environments
⇒ Full test suites compliant with IEEE 754-2008 standard.
⇒ Technical documentation
⇒ HDL core specification
⇒ Synthesis scripts
⇒ IP Core implementation support

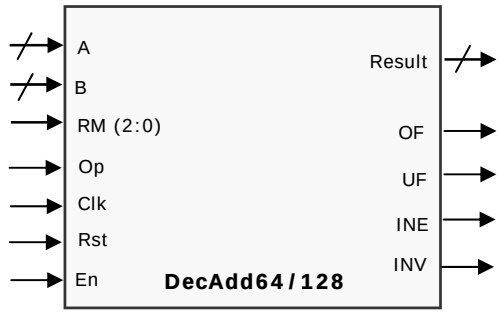
Configurations

DecAdd64/128 can be combined with other SilMinds IP core units to comprise arbitrary decimal coprocessor architectures. Deployment is made easy and reliable through a compact core size, parameterized RTL, and flexible test benches.

Product Verification

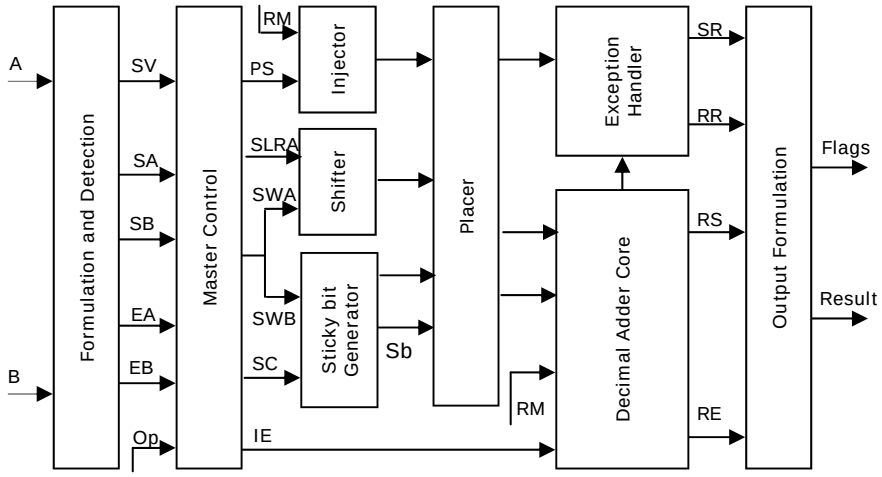
This product has been verified using an innovative and efficient constraint driven test vector generation tool. The test vectors cover all valid cases in conformance with the IEEE 754-2008 standard.

Symbol & Block Diagram



Inputs	
A, B	Augend and addend
RM	Rounding Mode
Op	Operation
Clk	System Clock
Rst	System Reset
En	Enable

Outputs	
Result	Resultant
OF	Overflow Flag
UF	Underflow Flag
INEF	INExact Flag
INVF	INValid Flag



A, B	Augend, Addend
RM	Rounding Mode
SA, SB	Significands A and B
EA, EB	Exponents A and B
SV	Special Values
SWA, SWB	Swapped A,B
SLRA	Shift Left/Right Amount
PS	Predicted Sign
IE	Intermediate Exponent
Sb	Sticky Bit
RR	Rounded Result
RE	Rounded Exponent
RS	Result Sign
SR	Special Result

Adder Unit Functions

Formulation & Detection

- Decodes input operands (Augend and Addend) using IEEE 754-2008 format to produce the sign bit, significand, and exponent
- Performs special input detection

Master Control

- Determines if operand swapping is needed
- Computes shift amounts for both operands
- Computes how many sticky counter digits will be collected in the sticky bit
- Encodes special values and passes them to the output formulation

Sticky-bit Generator

Determines the Sticky bit that results from logically ORing the bits of the digits to the right of the round digit

Shifter

Aligns the operands to reach the preferred exponent

Injector

Performs insertion of special digits into the smallest operand, before addition, to get the appropriate rounded result

Placer

Performs operands placement depending on the effective operation (subtraction or addition)

Decimal Adder Core

Performs decimal fixed point addition and subtraction; addition occurs in parallel at digit level; carry signals are propagated through a flagged Kogge-Stone prefix tree)

Exception Handler

Handles the exceptions and passes the special results to the output formulation unit

Output Formulation

- Encodes the resultant significand in DPD format
- Formulates the special values (infinity or NaN) to comply with the IEEE 754-2008 standard
- Sets the appropriate flags

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